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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/701,534	11/06/2003	James William Kretchmer	134765	8161
41838	7590	02/06/2006	EXAMINER	
GENERAL ELECTRIC COMPANY (PCPI)			LEE, HSIEN MING	
C/O FLETCHER YODER			ART UNIT	PAPER NUMBER
P. O. BOX 692289				2823
HOUSTON, TX 77269-2289				

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/701,534	KRETCHMER ET AL.
	Examiner	Art Unit
	Hsien-ming Lee	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 05 December 2005.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1,4-17 and 20-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1,4-13,15-17 and 20-27 is/are rejected.
- 7) Claim(s) 14 is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) All    b) Some \* c) None of:  
1. Certified copies of the priority documents have been received.  
2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**HSIEN-MING LEE**  
**PRIMARY EXAMINER**

2/2/06

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4, 5, 7, 10-13, 15-17, 20 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Witek et al. (US 6,146,970).

In re claims 1 and 11, Witek et al. teach a method for optical and electrical isolation between adjacent integrated devices, the method comprising:

- forming at least one trench 210 through an exposed surface of a silicon carbide semiconductor wafer 202 (col. 6, lines 8-11) by removing a portion of the semiconductor wafer material (Fig.6);
- forming an electrically insulating layer 212 (i.e. silicon oxide, col. 6, lines 56-57) on the sidewalls and the bottom of the at least one trench 210 (Fig.7);
- filling the at least one trench 210 by conformally depositing an optically isolating material 216a (i.e. an oxide, which is an opaque material or optically isolating material) and 218a (i.e. a nitride, which is an opaque material or optically isolating material) (Figs. 9 and 11); and
- planarizing the semiconductor wafer surface by removing the portion of the optically isolating material 216a and 218a above the exposed surface of the semiconductor wafer (Figs.9 and 12).

Art Unit: 2823

In re claims 4 and 5, Witek et al. teach forming an electrically insulating layer 212 comprising thermally growing a silicon oxide (col. 6, lines 56-57) on the sidewalls and the bottom of the at least one trench 210 .

In re claim 7, Witek teach that the optically isolating material 216a and 218a comprises an opaque material capable of being deposited conformally.

In re claim 10, Witek et al. teach that the optically isolating material (i.e. trench fill material) can be polysilicon (col. 11, lines 16-17).

In re claim 12, Witek et al. teach that the at least trench 210 is located between a plurality of adjacent device sites 220/230/240 (Fig.14).

In re claim 13, Witek et al. teach that forming the trench 210 comprises selectively etching the semiconductor wafer 202 with RIE (col. 6, lines 47-49).

In re claims 15 and 16, Witek teach planarizing the semiconductor wafer by subjecting the portion of the optically isolating material 216a and 218a above the exposed surface of the semiconductor wafer to an etching process, i.e. CMP (col. 7, lines 33-34 and col. 8, lines 30-32).

In re claim 17, Witek et al. teach a microelectronic device, comprising:

- at least two integrated devices 220 and 230, wherein the two integrated devices 220 and 230 are located in a silicon carbide substrate (Fig.14);
- at one trench 210 in the substrate 202, wherein the trench 210 physically separates the at least two integrated devices 220 and 230, and the inside of the at least 210 is coated with an electrically insulating, material 212 and filled with an optically isolating material 216c and 218b that is conformally deposited and followed by etching.

In re claim 20, Witek et al. teach that the electrically insulating layer 212 is a thermally grown silicon oxide (col. 6, lines 56-57).

In re claim 27, Witek et al. teach that the isolation structure is for MOSFET (col. 8, lines 50-56).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witek et al. in view of Pallinti et al. (US 6,607,967).

Witek et al do not teach that the electrically insulating layer is silicon nitride.

Pallinti et al. teach that using silicon nitride as a trench liner, which is equivalent to the electrically insulating layer, prior to filling the trench with trench filler material. The purpose of using silicon nitride as the trench liner is to function as an etch stop (col. 4, lines 31-35).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to use silicon nitride as taught by Pallinti et al., in the method of Witek et al., since by this manner it would provide an electrically insulating layer having etch-stop function, which in turn is advantageous to the subsequent CMP processing step.

5. Claims 8, 9, 21, 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witek et al. in view of Guo (US 6,894,357).

In re claims 9, 21 and 23, Witek et al. teach that the optically isolating material (i.e. trench fill material) can be polysilicon (col. 11, lines 16-17) but do not disclose that the polysilicon is formed by LPCVD.

However, using LPCVD for forming polysilicon has been widely used in the art, as evidenced by Guo (col. 6, lines 10-13 and 25-26).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to utilize LPCVD as taught by Guo to form polysilicon in Witek et al, since LPCVD is a good candidate for the purpose.

In re claims 8 and 24, Guo also remedy the deficiency in Witek et al. because the temperature in LPCVD is between 500 and 700 degrees C, which allows slightly below 500 degrees C.

In re claims 25 and 26, teachings of Witek et al. are illustrative rather than restrictive. One of the ordinary skill in the art would have been motivated to apply the teachings to any semiconductor devices that needs trench isolation to separate semiconductor devices.

***Allowable Subject Matter***

5. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record neither teaches nor suggests *oxidizing* the portion of the optically isolating material above the exposed surface of the semiconductor wafer and *removing the oxidized portion* of the optically isolating material.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (7:30 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee  
Primary Examiner  
Art Unit 2823

Feb. 2, 2006

HSIEN-MING LEE  
PRIMARY EXAMINER

2/2/06